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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants/ Appellants:	Gil Sih; Yushi Tian	Confirmation No.	9617
Serial No.:	10/006,044	Customer No.:	23696
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Docket No.:	010264	Group Art Unit:	2676
Title:	PROCESSING DIGITAL VIDEO DATA		

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450,
Alexandria, VA 22313

Dear Sir:

This is an Appeal Brief responsive to the final Office Action mailed August 22, 2005 and Advisory Action mailed March 21, 2006. The Notice of Appeal was filed on February 22, 2006. This Appeal Brief is being submitted in triplicate. Please charge Deposit Account No. 17-0026 for $620.00 ($500.00, as required by 37 C.F.R. §41.37(a)(2) and $120.00 for a one-month extension of time under 37 C.F.R. §1.17(a)(1)). Please also charge any additional fees that may be required or credit any overpayment to Deposit Account No. 17-0026.

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TABLE OF CONTENTS

REAL PARTY IN INTEREST

The real party in interest is Qualcomm, Incorporated, of San Diego, California.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1-5, 7-20, 23-26, 28-35 and 37-38 are on appeal in this case.

Claims 1-3 stand rejected under 35 U.S.C. §102(b) as being anticipated by McGuiness (U.S. Patent 6,104,416).

Claims 4-5, 7-20, 23-26, 28-35 and 37-38 stand rejected under 35 U.S.C. §103(a) as being unpatentable over McGuiness in view of Kohn (U.S. Patent No. 6,335,950).

Claims 23-26 and 28 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for lack of antecedent basis.

Claims 6, 21, 22, 27, and 36 have been canceled.

STATUS OF AMENDMENTS

The application was originally filed with claims 1-38. Claims 2-8, 10-16, 18, 29-30, 32-35, and 37-38 have never been amended.

Appellants amended claims 1, 9, 17-20, 25, 26, 31 and cancelled claims 6, 21, 22, 27 and 36 in the Response to the Non-Final Office Action mailed March 18, 2005.

Appellants amended claims 23-26 and 28 in the Response to the final Office Action mailed August 22, 2005. This after-final Amendment was entered in the Advisory Action mailed March 21, 2006.

SUMMARY OF THE INVENTION

In general, the Appellants' invention is directed to techniques that facilitate the processing of multi-dimensional blocks of digital video data.[1] Discrete blocks of video data are commonly used for video coding according to any of a wide variety of video coding standards, such as the different MPEG standards and others.[2] In such cases, motion estimation and motion compensation can be performed to encode the data and exploit redundancy across multiple frames of a video sequence. The claimed invention is defined in terms of methods, systems and devices that implement the techniques.[3]

More specifically, the claimed invention provides a video direct memory access (VDMA) controller that supports a unique command for directly accessing blocks of video data in an efficient manner.[4] The command may improve the ability to encode and decode multidimensional blocks of video data.[5] In particular, according to the claimed invention, a single command causes the VDMA controller to access storage units of a memory and fetch a multidimensional block of video data from multiple non-contiguous rows of the memory in response to the command.[6] In this manner, the VDMA controller can access a multi-dimensional block of video data without having to perform a high number of address calculations.[7]

By using the unique command defined by the claimed invention, and a corresponding VDMA controller architecture to support the unique command, components of a coding device can write and read video data more efficiently.[8] In particular, as mentioned above, the components can access a block of video data without having to perform the high number of address calculations that is typically required to access video data. A high number of address calculations is ordinarily needed due to the non-sequential manner in which video data is typically stored.[9]

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[1] See Application at paragraph [0006].
[2] See Application at paragraphs [0003] and [0005].
[3] See all pending claims.
[4] See Application at paragraph [0033].
[5] Id.
[6] See independent claim 1, independent claim 9, independent claim 17 and independent claim 31.
[7] See Application at paragraph [0021].
[8] See Application at paragraph [0033].
[9] See Application at paragraph [0021].

The invention also contemplates several specific features and parameters of the unique VDMA command.[10] For example, the command may specify a number of rows and a number of columns for the block of video data that is stored in non-contiguous rows of the memory.[11] Also, the command may specify a jump parameter, indicating a number of storage units between each row of the video block.[12] The VDMA controller is designed to support the command having these parameters in order to provide for efficient fetches of multi-dimensional video blocks.

In particular, the command can be executed in the VDMA controller, and based on the parameters of the command, the VDMA controller fetches an entire multi-dimensional block of video data from non-contiguous rows of memory. For example, address generation logic can be designed to automatically jump to addresses in non-contiguous rows of the memory according to the jump parameter, without requiring address calculations commonly needed in conventional systems.[13]

[10] See e.g., Application at paragraph [0035].
[11] Id. See also, e.g., claim 2.
[12] Id. See also, e.g., claim 3.
[13] See e.g., Application at paragraph [0053]

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Appellants submit the following grounds of rejection to be reviewed on Appeal:

(1) The first ground of rejection to be reviewed on Appeal is the rejection of claims 1-3 under 35 U.S.C. §102(b) as being anticipated by McGuiness.

(2) The second ground of rejection to be reviewed on Appeal the rejection of claims 4-5, 7-20, 23-26, 28-35, 37, and 38 under 35 U.S.C. §103(a) as being unpatentable over McGuiness in view of Kohn.

(3) The third ground of rejection to be reviewed on Appeal is the rejection of claims 23-26 and 28 under 35 U.S.C. §112 as being indefinite for lack of antecedent basis.

ARGUMENTS

The final Office Action rejected claims 1-3 under 35 U.S.C. §102(b) as being anticipated by McGuiness (US 6,104,416) and rejected claims 4-5, 7-20, 23-26, 28-35, 37, and 38 under 35 U.S.C. §103(a) as being unpatentable over McGuiness (US 6,104,416) in view of Kohn (US 6,335,950). In addition, the final Office Action rejected claims 23-26 and 28 under 35 U.S.C. §112 as being indefinite for lack of antecedent basis.

The McGuiness Reference

The McGuiness reference is the primary reference used in the rejections of all pending claims. The final Office Action and the advisory Office Action indicated that McGuiness discloses a command that causes a programmable VDMA controller to fetch a multidimensional block of video data from multiple non-contiguous rows of the memory. However, the interpretation of McGuiness in the final Office Action is erroneous. McGuiness does not disclose or suggest any command that causes a programmable VDMA controller to fetch a multidimensional block of video data from multiple non-contiguous rows of the memory

Indeed, nowhere in McGuiness is there any discussion of a command that causes a fetch of a multidimensional block of video data from non-contiguous rows in memory. On the contrary, McGuiness requires multiple commands to fetch a block of video data. Furthermore, to the extent that McGuiness describes memory "bursts" that may access multiple rows of a tile, the multiple rows of the tile are stored in a <u>contiguous</u> fashion.

FIG. 7 of McGuiness was cited in the final Office Action, and is reproduced below.

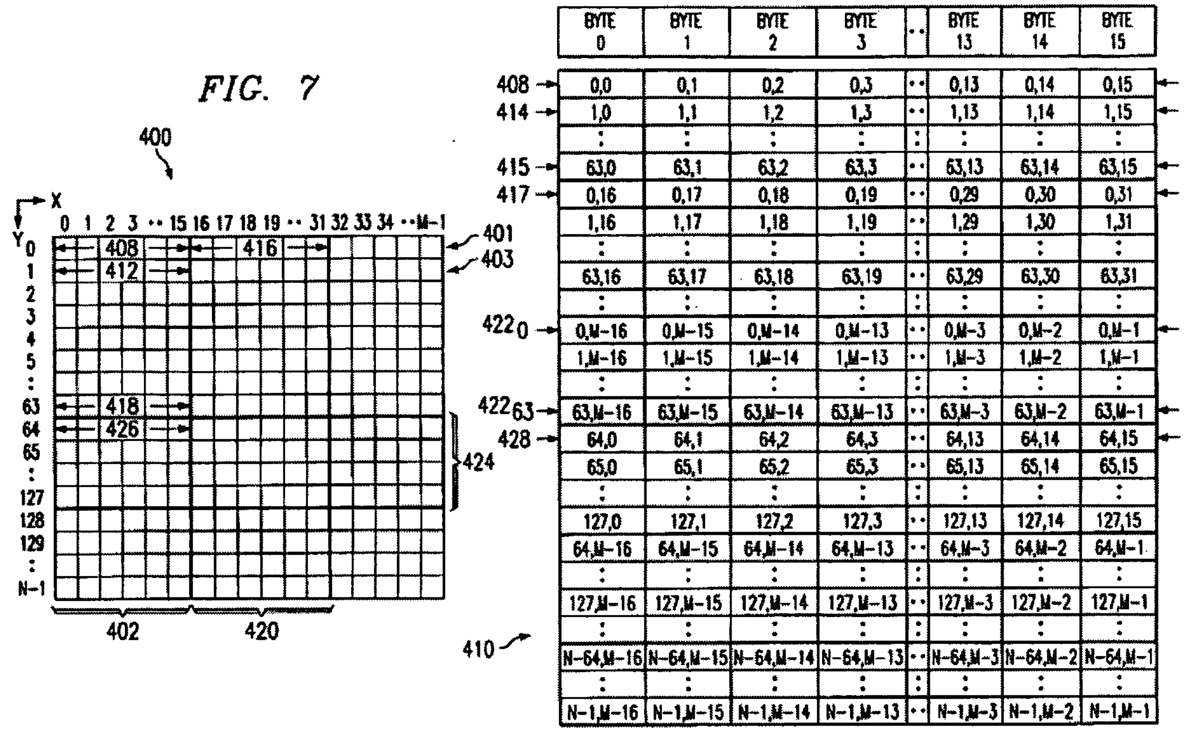

FIG. 7

The final Office Action cited FIG. 7 and the corresponding description as describing a process of loading several rows of video data. In the McGuiness discussion, however, each row of the video data is assigned a unique "word address" in memory. In particular, as described by McGuiness in the discussion of FIG. 7:

> All of the pixels in the first row 406 of the first tile 402 are read by reading a first word 408 of the memory 410.[14]

Furthermore, McGuiness indicates that:

> The next row 403 is read by repeating the above process starting by reading word 414 having a word address of the first word, plus one.[15]

From these passages, it is clear that McGuiness is not using a single command to fetch a multidimensional block of video data, whatsoever, much less fetch from multiple non-contiguous rows of the memory. Instead, McGuiness describes separate word addresses that are "repeated" row-by-row in order to fetch video data. In other words, each row has a different word address, requiring <u>multiple</u> word addresses to fetch a

[14] McGuiness at column 12, lines 34-36.
[15] McGuiness at column 12, lines 46-48.

multidimensional block of data. This is in contrast to the claimed invention, which requires a single command.

Moreover, all data fetched from memory by the McGuiness system is stored in contiguous rows of memory. Indeed, the teaching of McGuiness does not appear to be concerned with reading non-contiguous rows of memory, whatsoever, as required by Appellants' claims. Instead, McGuiness appears to be rearranging a video image such that a video "tile" is stored in contiguous memory. Therefore, contrary to the claimed invention, McGuiness lacks a single command to fetch a multidimensional block from non-contiguous rows.

The final Office Action seems to be arguing that McGuiness teaches a "burst" that fetches more than one row of a given tile. However, a burst is not necessarily one command, and actually uses several successive commands. Moreover, even if McGuiness allows a single "burst" to fetch more than one row of a given tile, the burst would still fetch from contiguous rows of memory (rather than from non-continuous rows of memory as required by Appellants' claims).[16] See column 9, lines 1-10. Furthermore, at column 10, lines 59-66, McGuiness also indicates that with respect to FIG. 7:

> A location in memory is selected as the first word 408, and the data in the first row 406 of the first tile 402 of the picture, is stored in the first word 408. The data in a subsequent row 412 of the first tile is stored in the next word 414. This is continued until the last row 418 of the tile. Storing a row of the tile 402 in a word directly after the word that stores the preceding row of the tile 402 enables easy retrieval of the rows in a single burst.[17]

In clear contrast to McGuiness, which rearranges the storing of video data to store contiguous in a linear fashion, Appellants' claimed techniques allow single command access to a multi-dimensional block of video data that is stored in non-contiguous rows of memory. In particular, Appellants' claims require a command that specifies a multidimensional block of video data and fetches the multidimensional block of video data from multiple non-contiguous rows of the memory. Nothing in McGuiness suggests a command that fetches anything from non-contiguous rows of the memory. Instead, McGuiness teaches tile re-arrangement in a manner that may allow bursts to contiguous rows of the memory to fetch a tile.

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[16] See McGuiness at column 9, lines 1-10.
[17] McGuiness at column 10, lines 59-66.

The Kohn Reference

The Kohn reference is a secondary reference used in the final Office Action in the obviousness rejections. Essentially, the final Office Action cited Kohn as teaching various features of Appellants' dependent claims, and argued that a person of ordinary skill in the art would have been motivated to modify the system of McGuiness in view of the teaching of Kohn.

Nothing in the Kohn reference provides any teaching that would remedy the deficiencies of McGuiness with respect to Appellants' independent claims. In particular, the Kohn reference, like the McGuiness reference, lacks any suggestion of a single command that causes a fetch of a multi-dimensional block of video data from non-contiguous rows of the memory.

Moreover, many of the observations in the final Office Action regarding the Kohn reference are erroneous. With respect to dependent claim 5, for example, the final Office Action indicated that Kohn teaches transferring a block of video data from a source memory to a destination memory.[18] Based on this, the final Office Action then stated "it is implied that the destination memory is specified with a starting address."[19] Nothing in the cited passage of Kohn, however, discloses or suggests a single command that specifies a starting address of the video block within the memory, and a starting address within the destination memory, as required by claim 5.

FIRST GROUND OF REJECTION UNDER APPEAL - Claims 1-3

Claims 1-3 stand rejected under rejected under 35 U.S.C. §102(b) as being anticipated by McGuiness. In order to support an anticipation rejection under 35 U.S.C. §102, it is well established that a prior art reference must disclose each and every element of a claim. This well known rule of law is commonly referred to as the "all-elements rule."[20] If a prior art reference fails to disclose any element of a claim, then rejection under 35 U.S.C. §102 is improper.[21] In the current case, one or more

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[18] See final Office Action, page 5, lines 5-6.
[19] See final Office Action, page 5, lines 6-7.
[20] *See Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 USPQ 81 (CAFC 1986) ("it is axiomatic that for prior art to anticipate under 102 it has to meet every element of the claimed invention").
[21] *Id. See also Lewmar Marine, Inc. v. Barient, Inc.* 827 F.2d 744, 3 USPQ2d 1766 (CAFC 1987); *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (CAFC 1990); *C.R. Bard, Inc. v. MP Systems, Inc.*, 157 F.3d

features of claims 1-3 are not disclosed or suggested in McGuiness. Therefore, the rejections must be reversed.

Group 1 - Claim 1

Independent claim 1 recites a system comprising a memory having linearly addressable storage units to store video data, and a programmable video direct memory access (VDMA) controller to access the storage units of the memory in response to a command specifying a multidimensional block of video data and fetch the multidimensional block of video data from multiple non-contiguous rows of the memory in response to the command.

The final Office Action indicated that McGuiness teaches a command that causes a programmable VDMA controller to fetch a multidimensional block of video data from multiple non-contiguous rows of the memory. However, McGuiness does not suggest such a command. Instead, McGuiness describes a system in which multiple commands are executed to fetch a multidimensional block of video data. Moreover, all data fetched in the McGuiness system are from contiguous rows.

To the extent that McGuiness teaches the use of a signal memory "burst" (which is not necessarily one command) to access multiple rows from memory, the multiple rows accessed by such a memory burst are arranged in a contiguous fashion in the memory. Therefore, even if the memory burst of McGuiness were construed as a single command, McGuiness still does not suggest the fetching of video data that is stored in <u>non-contiguous</u> rows of memory, as required by the claims. In fact, McGuiness does not teach or suggest the fetching of any data from memory that is non-contiguous, much less a command that causes a programmable VDMA controller to fetch a multidimensional block of video data from multiple non-contiguous rows of the memory.

A single command that causes a programmable VDMA controller to fetch a multidimensional block of video data from multiple non-contiguous rows of the memory can simplify read and write operations during video encoding by reducing or eliminating a high number of address calculations that would otherwise be necessary to locate the multidimensional block of video data stored in the non-contiguous rows

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1340, 48 USPQ2d 1225 (CAFC 1998); *Oney v. Ratliff*, 182 F.3d 893, 51 USPQ2d 1697 (CAFC 1999); *Apple Computer, Inc. v. Articulate Systems, Inc.*, 234 F.3d 14, 57 USPQ2d 1057 (CAFC 2000).

of the memory. Again, the system of McGuiness, in contrast to the features of Appellants' claims, appears to require multiple commands to fetch a multidimensional block of video data from non-contiguous rows, and only contemplates memory bursts that may fetch multiple contiguous rows (rather than non-contiguous rows).

In short, McGuiness provides absolutely no discussion of a command that causes a fetch of a multidimensional block of video data from non-contiguous rows in memory. On the contrary, McGuiness appears to require multiple commands to fetch a block of video data. Furthermore, to the extent that McGuiness describes memory "bursts" that may access multiple rows of a tile, the multiple rows of the tile are stored in a contiguous fashion.

In the McGuiness discussion, each row of the video data is assigned a unique "word address" in memory. Again, as described by McGuiness:

> All of the pixels in the first row 406 of the first tile 402 are read by reading a first word 408 of the memory 410.[22]

Furthermore, McGuiness indicates that:

> The next row 403 is read by repeating the above process starting by reading word 414 having a word address of the first word, plus one.[23] See column 12, lines 46-48.

From these passages, it is clear that McGuiness does not suggest the use of a signal command to fetch a multidimensional block of video data, whatsoever, much less fetch from multiple non-contiguous rows of the memory. Instead, McGuiness describes separate word addresses that are "repeated" row by row in order to fetch video data.

Moreover, all data fetched from memory by the McGuiness system is stored in contiguous rows of memory. Indeed, the teaching of McGuiness does not appear to be concerned with reading non-contiguous rows of memory, as required by Appellants' claims. Instead, McGuiness appears to be rearranging a video image such that a video "tile" is stored in contiguous memory. Therefore, even if McGuiness allows a single "burst" to fetch more than one row of a given tile, the burst would still fetch from contiguous rows of memory (rather than from non-continuous rows of memory as required by Appellants' claims).

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[22] McGuiness at column 12, lines 34-36.
[23] McGuiness at column 12, lines 46-48.

At column 10, lines 59-66, McGuiness also indicates that with respect to FIG. 7:

> A location in memory is selected as the first word 408, and the data in the first row 406 of the first tile 402 of the picture, is stored in the first word 408. The data in a subsequent row 412 of the first tile is stored in the next word 414. This is continued until the last row 418 of the tile. Storing a row of the tile 402 in a word directly after the word that stores the preceding row of the tile 402 enables easy retrieval of the rows in a single burst.[24] Column 10, lines 59-66.

In contrast to McGuiness, which rearranges the storing of video data and accesses contiguous rows of a tile, Appellants' claimed techniques allow single command access to a block of video data that is stored in non-contiguous fashion. In particular, Appellants' claims require a command that specifies a multidimensional block of video data and fetches the multidimensional block of video data from multiple non-contiguous rows of the memory. Nothing in McGuiness suggests a command that fetches anything from non-contiguous rows of the memory. Instead, McGuiness teaches tile re-arrangement in a manner that may allow bursts to contiguous rows of the memory to fetch a tile.

Since nothing in McGuiness suggests a command that fetches video data from non-contiguous rows of a memory, all pending rejections that rely on McGuiness are deficient. Furthermore, nothing in the Kohn reference provides any teaching that would remedy the deficiencies of McGuiness outlined above. In particular, the Kohn reference, like the McGuiness reference, lacks any suggestion of a single command that causes a fetch of a multi-dimensional block of video data from non-contiguous rows of the memory.

Group 2 - Claim 2

Claim 2 is dependent upon claim 1, and stands rejected under 35 U.S.C. §102(b) as being anticipated by McGuiness. Claim 2 is separately patentable from claim 1 and does not stand or fall with claim 1.

Claim 2 requires the command to specify a number of rows and a number of columns for the block of video data. Thus, claim 2 requires the command to specify a number of rows and a number of columns for the block of video data, and in response

[24] McGuiness at column 10, lines 59-66.

to this command the VDMA controller must access the storage units of the memory in response to a command specifying a multidimensional block of video data and fetch the multidimensional block of video data from multiple non-contiguous rows of the memory. This feature of claim 2 is also lacking from McGuiness, particularly in the context of the features of independent claim 1.

Group 3 - Claim 3

Claim 3 is dependent upon claim 1, and stands rejected under 35 U.S.C. §102(b) as being anticipated by McGuiness. Claim 3 is separately patentable from claim 1 and does not stand or fall with claim 1.

Claim 3 requires the command to specify a jump parameter indicating a number of storage units between each row of the video block. Thus, claim 3 requires the command to specify a number of rows and a number of columns for the block of video data, and in response to this command the VDMA controller must access the storage units of the memory in response to a command specifying a multidimensional block of video data and fetch the multidimensional block of video data from multiple non-contiguous rows of the memory in response to the command. The feature of claim 3 is lacking from McGuiness, particularly in the context of the features of independent claim 1.

The final Office Action indicated that, in McGuiness, pixels of a first row 416 of the next tile are read by reading word 417 at the word address of the first word 408 plus X. The final Office Action indicated that X is a jump parameter.

Nothing in McGuiness, however, suggests a command that specifies a jump parameter "X," such that a VDMA controller uses the jump parameter to access multiple non-contiguous rows. To be sure, in the analysis of the final Office Action, the first and second words of 417 are contiguous and form part of the same row. Moreover, nothing in McGuiness suggests that multidimensional block of video data from multiple non-contiguous rows, much less a jump parameter of a single command to facilitate fetching of such data from non-contiguous rows. Nor would it have been obvious to modify McGuiness to include a jump parameter insofar as there is no prior art teaching applied in the final Office Action that suggests this feature.

SECOND GROUND OF REJECTION UNDER APPEAL - Claims 4-5, 7-20, 23-26, 28-35, 37, and 38.

Claims 4-5, 7-20, 23-26, 28-35, 37, and 38 stand rejected under 35 U.S.C. §103(a) as being unpatentable over McGuiness in view of Kohn. These rejections, however, are improper for essentially the same reasons that the rejections of claims 1-3 are improper under 35 U.S.C. §103(a). In particular, the McGuiness reference lacks any teaching or suggestion of a single DMA command that facilitates access to a multidimensional block of video data stored in non-contiguous rows of a memory. Moreover, the Kohn reference lacks any teaching that would remedy this basic deficiency of McGuiness with respect to the independent claims.

In order to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.[25] The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in Appellants' disclosure.[26]

In the current case, neither the McGuiness reference nor the Kohn reference provides any teaching or suggestion of a single DMA command that facilitates access to a multidimensional block of video data stored in non-contiguous rows of a memory. For this reason, rejections of all pending claims must be reversed.

Group 4 - Independent claims 9, 17 and 31

The rejections of claims 9 17 and 31 must be reversed for essentially the same reason that the rejection of claim 1 under 35 U.S.C. 102(b) must be reversed. Namely, the final Office Action is based on a misinterpretation of the McGuiness reference. Nothing in McGuiness discloses or suggests the features attributed to this reference in the final Office Action.

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[25] See MPEP 2143.

[26] Id citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

Independent claim 9 recites a method comprising receiving a direct memory access (DMA) command from a processor to transfer a multidimensional block of video data, generating a set of source addresses and a set of destination addresses for the multidimensional block of video data in response to the command, wherein the set of source addresses correspond to multiple non-contiguous rows of a source memory, and copying video data from the source memory to a destination memory according to the source addresses and destination addresses in response to the command.

Independent claim 17 recites a device comprising a first memory to store a candidate video block to be encoded, a second memory to store a set of video data blocks from which to encoded the candidate video block, a differential calculator to calculate differential metrics between the candidate video block and the set of video blocks; and a programmable video direct memory access (VDMA) controller to copy the candidate video block and the set of video blocks from a video memory to the first memory and the second memory, respectively, wherein the VDMA controller copies the set of blocks to the second memory in response to a single direct memory access (DMA) command specifying a multidimensional search space of video data stored within the video memory in multiple non-contiguous rows.

Independent claim 31 recites a device comprising means for receiving a direct memory access (DMA) command from a processor to transfer a multidimensional block of video data, means for generating a set of source addresses and a set of destination addresses for the multidimensional block of video data in response to the command, wherein the set of source address correspond to multiple non-contiguous rows of a source memory, and means for copying video data from the source memory to a destination memory according to the source addresses and destination addresses.

The final Office Action stated the following:

> McGuiness teaches a method of retrieving a block of video data from a linearly addressable memory in response to a DMA command, including generating a set of addresses corresponding to multiple non-contiguous rows of a source memory, and the addresses generated including specifying a number of rows and columns, and also teach specifying a jump parameter indicating the number of addresses between each row of the video block. McGuiness also teaches a motion estimation unit having an internal memory. Thus, McGuiness et al. teach all the limitations of claims 9-16, 31-35, 37-38 except for copying a video data from a source memory to a destination memory according to a source addresses and destination addresses, and except

> for receiving the command via a first bus, and receiving a command via a second bus.[27]

Also, with respect to claims 17-20, 23-26 and 28-30, the final Office Action re-stated the passage above, but noted that McGuiness lacks teaching of:

> the copying of video data from a source memory to a destination memory according to source addresses and destination addresses; receiving the command via a first bus, and receiving a second command via a second bus; and a command buffer to store search commands.[28]

The interpretations of McGuiness in the final Office Action are clearly erroneous. McGuiness does not teach the features attributed to this reference in the final Office Action. For example, as outlined above, McGuiness does not teach or suggest any command that causes fetching of video data that is stored in non-contiguous rows of memory, as required by the claims.

More specifically, with respect to claim 9, McGuiness does not disclose or suggest a command that causes generation of a set of source addresses and a set of destination addresses for the multidimensional block of video data, wherein the set of source addresses correspond to multiple non-contiguous rows of a source memory.

With respect to claim 17, McGuiness does not disclose or suggest a single command that causes a VDMA controller to copy a set of blocks from a first memory to a second memory, wherein the single command specifies a multidimensional search space of video data stored within the video memory in multiple non-contiguous rows.

With respect to claim 31 McGuiness does not disclose or suggest a means for generating a set of source addresses and a set of destination addresses for the multidimensional block of video data in response to a command, wherein the set of source address correspond to multiple non-contiguous rows of a source memory.

These features are simply lacking from the disclosure of McGuiness. Again, McGuiness executes multiple commands to fetch a multidimensional block of video data, and moreover, the fetches performed by McGuiness are not from non-contiguous rows. On the contrary, multidimensional video block data fetches in McGuiness involve multiple executed commands that fetch from contiguous rows.

[27] Final Office Action, page 5, lines 13-22.
[28] Final Office Action, page 6, lines 10-19.

Nothing in the Kohn reference provides any teaching that would remedy the deficiencies of McGuiness with respect to Appellants' independent claims. In particular, the Kohn reference, like the McGuiness reference, lacks any suggestion of a single command that causes a fetch of a multi-dimensional block of video data from non-contiguous rows of the memory.

Group 5 - Dependents claims 5, 13, 26 and 35

Claims 5, 13, 26 and 35 are dependent claims that require the command (causes fetching of video data that is stored in non-contiguous rows of memory) to specify a starting address of the video block within the memory and a starting address within a destination memory. Claims 5, 13, 26 and 35 are separately patentable from the respective independent claims and do not stand or fall with the independent claims.

The final Office Action acknowledged that this feature is lacking from McGuiness. However, the final Office Action indicated that Kohn teaches transferring a block of video data from a source memory to a destination memory.[29] Based on this, the final Office Action then states "it is implied that the destination memory is specified with a starting address."[30]

Nothing in the cited passage of Kohn, however, discloses or suggests a single command that specifies a starting address of the video block within the memory, and a starting address within the destination memory. Accordingly, the rejections of claims 5, 13, 26 and 35 should be reversed for this additional reason.

Group 6 - Dependents claims 11, 23 and 33

Claims 11, 23 and 33 are dependent claims that require the command (causes fetching of video data that is stored in non-contiguous rows of memory) to specify a number of rows and columns for the block of video data. Claims 11, 23 and 33 are separately patentable from the respective independent claims and do not stand or fall with the independent claims.

The final Office Action attributed the features of claims 11, 23 and 33 to McGuiness without citing any passage of this reference. However, McGuiness lacks

[29] See final Office Action, page 5, lines 5-6.
[30] See final Office Action, page 5, lines 6-7.

any suggestion of a command that specifies a number of rows and columns for the block of video data, much less a command that causes fetching of video data that is stored in non-contiguous rows of memory, as further required by the respective independent claims.

For this additional reason, it is clear that McGuiness lacks any suggestion of a command that specifies a number of rows and columns for the block of video data. Therefore, the rejections of claim 11, 23 and 33 should be reversed.

Group 7 - Dependents claims 8, 16 and 38

Claims 8, 16 and 38 are dependent claims that require a motion estimation unit having an internal memory and a differential calculator to calculate a distortion metric between blocks of video data, wherein the VDMA controller copies blocks of video data from the memory to the internal cache of the motion estimation unit in response to the command (which causes fetching of video data that is stored in non-contiguous rows of memory). Claims 8, 16 and 38 are separately patentable from the respective independent claims and do not stand or fall with the independent claims.

The final Office Action attributed the features of claims 8, 16 and 38 to McGuiness, once again, without citing any passage of this reference. Appellants have conducted an electronic search of the McGuiness reference for the term "estimation" and "motion estimation" and this reference does not even use these terms. Nor have Appellants found any similar terminology. Therefore, the comments in the final Office Action that McGuiness suggests a motion estimation unit having an internal memory appears to be pure conjecture.

For this additional reason, it is clear that McGuiness lacks any suggestion of a motion estimation unit having an internal memory. Therefore, the rejections of claim 11, 23 and 33 should be reversed. Appellants note that this feature essentially requires the fetching of the multidimensional block of video data from multiple non-contiguous rows of the first memory to load such video data into the internal memory (cache) of the a motion estimation unit, which is clearly not taught by any of the applied references.

Group 8 - Dependents claims 12, 25 and 34

Claims 12, 25 and 34 are dependent claims that require the command that causes fetching of a multidimensional block of video data from non-contiguous rows to include a jump parameter indicating a number of storage units between each row of the video block. Thus, claims 12, 25 and 34 require the command to specify a jump parameter, and the VDMA controller must access the storage units of the memory in response to the command and fetch a multidimensional block of video data from multiple non-contiguous rows of the memory. Claims 12, 25 and 34 are separately patentable from the respective independent claims and do not stand or fall with the independent claims.

The final Office Action attributed the features of claims 12, 25 and 34 to McGuiness. However, McGuiness lacks any suggestion of a command that includes a jump parameter for accessing data from multiple non-contiguous rows.

In the analysis of claim 3, the final Office Action indicated that, in McGuiness, pixels of a first row 416 of the next tile are read by reading word 417 at the word address of the first word 408 plus X. The final Office Action indicated that X is a jump parameter.

Nothing in McGuiness, however, suggests a command that specifies a jump parameter "X," such that a VDMA controller uses the jump parameter to access multiple non-contiguous rows. To be sure, in the analysis of the final Office Action, the first and second words of element 417 are contiguous and form part of the same row. Moreover, nothing in McGuiness suggests that multidimensional block of video data from multiple non-contiguous rows, much less a jump parameter of a single command to facilitate fetching of such data from non-contiguous rows.

For this additional reason, it is clear that McGuiness lacks any suggestion of a command that includes a jump parameter for accessing data from multiple non-contiguous rows. Therefore, the rejections of claim 12, 25 and 34 should be reversed.

THIRD GROUND OF REJECTION UNDER APPEAL - Claims 23-26 and 28

The third ground of rejection to be reviewed on Appeal is the rejection of claims 23-26 and 28 under 35 U.S.C. §112, second paragraph, as being indefinite for lack of antecedent basis. This rejection was advanced in the final Office Action, and Appellants addressed these rejections in an after-final Amendment, which was entered according to the Advisory Action.

The Advisory Action, however, appeared to maintain all of the rejections of the final Office Action. This may have been an oversight in the Advisory Action. In any case, to the extent that claims 23-26 and 28 remain rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for lack of antecedent basis, Appellants request reversal of these rejections insofar as the after-final Amendment addressed any antecedent basis issues that may have existed in claims 23-26 and 28 prior to such amendment.

CONCLUSION OF ARGUMENTS

The final Office Action failed to establish anticipation with respect to claims 1-3. The final Office Action also failed to establish a prima facie case of obviousness with respect to claims 4-5, 7-20, 23-26, 28-35 and 37-38. Finally, all claim rejections under 35 U.S.C. 112, second paragraph, have been overcome. In view of Appellants' arguments, the final rejection of claims 1-5, 7-20, 23-26, 28-35 and 37-38 is improper and should be reversed.

Each of the eight different groupings of claims addressed above are separately patentable. Accordingly, the different groups do not necessarily stand or fall together.

Respectfully submitted,

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APPENDIX: CLAIMS ON APPEAL

Claim 1 (Previously presented): A system comprising:

a memory having linearly addressable storage units to store video data; and

a programmable video direct memory access (VDMA) controller to access the storage units of the memory in response to a command specifying a multidimensional block of video data and fetch the multidimensional block of video data from multiple non-contiguous rows of the memory in response to the command.

Claim 2 (Original): The system of claim 1, wherein the command specifies a number of rows and a number of columns for the block of video data.

Claim 3 (Original): The system of claim 1, wherein the command specifies a jump parameter indicating a number of storage units between each row of the video block.

Claim 4 (Original): The system of claim 1, wherein in response to the command, the VDMA controller copies the video data from the memory to a destination memory.

Claim 5 (Original): The system of claim 4, wherein the command specifies a starting address of the video block within the memory, and a starting address within the destination memory.

Claim 6 (Canceled).

Claim 7 (Original): The system of claim 1, further comprising:

a processor to issue commands to the VDMA controller via a first bus; and

a digital signal processor to issue commands to the VDMA controller via a second bus.

Claim 8 (Original): The system of claim 1, further comprising a motion estimation unit having an internal memory and a differential calculator to calculate a distortion metric between blocks of video data, wherein the VDMA controller copies blocks of

video data from the memory to the internal cache of the motion estimation unit in response to the command.

Claim 9 (Previously presented): A method comprising:

receiving a direct memory access (DMA) command from a processor to transfer a multidimensional block of video data;

generating a set of source addresses and a set of destination addresses for the multidimensional block of video data in response to the command, wherein the set of source addresses correspond to multiple non-contiguous rows of a source memory; and

copying video data from the source memory to a destination memory according to the source addresses and destination addresses in response to the command.

Claim 10 (Original): The method of claim 9, wherein the source memory and the destination memory each have linearly addressable storage units.

Claim 11 (Original): The method of claim 9, wherein the command specifies a number of rows and a number of columns for the block of video data, and wherein generating a set of addresses comprises calculating the source addresses and destination addresses as a function of the number of rows and the number of columns.

Claim 12 (Original): The method of claim 9, wherein the command specifies a jump parameter indicating a number of addresses between each row of the video block, and wherein generating a set of addresses comprises calculating the source addresses and destination addresses as a function of the jump parameter.

Claim 13 (Original): The method of claim 9, wherein the command specifies a starting source address of the video block within the source memory, and a starting destination address within the destination memory.

Claim 14 (Original): The method of claim 9, wherein copying video data comprises fetching an entire block of video data having multiple rows in response to the command.

Claim 15 (Original): The method of claim 9, wherein receiving the command comprises receiving the command via a first bus, the method further comprising receiving a second command from a digital signal processor via a second bus.

Claim 16 (Original): The method of claim 9, wherein copying video data comprises copying the video data to an internal cache of a motion estimation unit in response to the command.

Claim 17 (Previously presented): A device comprising:

a first memory to store a candidate video block to be encoded;

a second memory to store a set of video data blocks from which to encoded the candidate video block;

a differential calculator to calculate differential metrics between the candidate video block and the set of video blocks; and

a programmable video direct memory access (VDMA) controller to copy the candidate video block and the set of video blocks from a video memory to the first memory and the second memory, respectively, wherein the VDMA controller copies the set of blocks to the second memory in response to a single direct memory access (DMA) command specifying a multidimensional search space of video data stored within the video memory in multiple non-contiguous rows.

Claim 18 (Original): The device of claim 17, wherein the set of video data blocks stored by the second memory comprises a complete video data frame.

Claim 19 (Previously presented): The device of claim 17, wherein the differential calculator include address generation logic to read the candidate video block from the first memory and one or more video blocks of the set of video blocks from the second memory.

Claim 20 (Previously presented): The device of claim 19, wherein the differential calculator reads the candidate video block from the first memory and one or more video blocks of the set of video blocks from the second memory in parallel.

Claims 21-22 (Canceled).

Claim 23 (Currently amended): The device of claim 17~~22~~, wherein the command specifies a number of rows and a number of columns for the search space of video data.

Claim 24 (Currently amended): The device of claim 17~~21~~, wherein the video memory includes a plurality of linearly addressable storage units to store video data.

Claim 25 (Currently amended): The device of claim 17~~21~~, wherein the command specifies a jump parameter indicating a number of storage units between each row of the search space.

Claim 26 (Currently amended): The device of claim 17~~21~~, wherein the command specifies a starting source address of the search space within the video memory, and a starting destination address within the second memory.

Claim 27 (Canceled).

Claim 28 (Currently amended): The device of claim 17~~21~~, further comprising:

a processor to issue commands to the VDMA controller via a first bus; and

a digital signal processor (DSP) to issue commands to the VDMA controller via a second bus.

Claim 29 (Original): The device of claim 17, wherein the differential calculator calculates the differential metrics in response to search commands, and wherein each search command specifies a multidimensional region of video data stored within the second memory.

Claim 30 (Original): The device of claim 29, further comprising a command buffer to store the search commands and deliver the search commands to the differential calculator.

Claim 31 (Previously presented): A device comprising:

means for receiving a direct memory access (DMA) command from a processor to transfer a multidimensional block of video data;

means for generating a set of source addresses and a set of destination addresses for the multidimensional block of video data in response to the command, wherein the set of source address correspond to multiple non-contiguous rows of a source memory; and

means for copying video data from the source memory to a destination memory according to the source addresses and destination addresses.

Claim 32 (Original): The device of claim 31, wherein the source memory and the destination memory each have linearly addressable storage units.

Claim 33 (Original): The device of claim 31, wherein the command specifies a number of rows and a number of columns for the block of video data, and wherein the generating means comprises means for calculating the source addresses and destination addresses as a function of the number of rows and the number of columns.

Claim 34 (Original): The device of claim 31, wherein the command specifies a jump parameter indicating a number of addresses between each row of the video block, and wherein the generating means comprises means for calculating the source addresses and destination addresses as a function of the jump parameter.

Claim 35 (Original): The device of claim 31, wherein the command specifies a starting source address of the video block within the source memory, and a starting destination address within the destination memory.

Claim 36 (Canceled).

Claim 37 (Original): The device of claim 31, wherein the receiving means receives the command via a first bus and a second command from a digital signal processor via a second bus.

Claim 38 (Original): The device of claim 31, wherein the copying means comprises means for copying the video data to an internal cache of a motion estimation unit in response to the command.